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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	19

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/344,847	PANESAR, GAJINDER SINGH	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 1998* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicant's Response mailed on July 23, 2004. Claim 8 was amended. Claims 1-9 of the application are pending.

Drawings

2. The applicant has mentioned on Page 2 of the amendment of July 23, 2004 that Figure 7 has been amended as required in the previous Office Action to correct a typographical error and a replacement sheet and one amended sheet have been presented. However, USPTO has not received such a replacement sheet and one amended sheet.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA

1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1 and 2 of U.S. Patent No. 6,697,774. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Claim 1 teaches a method of operating a computer system to design an application specific processor (ASP) comprising:

defining a set of peripherals for the ASP which are responsive to stimuli and which communicate with a processor;

generating for each peripheral an input file which defines the functional attributes of that peripheral in a high level language with an input data structure;

entering the input file into the computer system and operating a modelling tool loaded on the computer system to generate from the input file a register definition file by allocating specific elements of the input data structure to predefined sectors of a register definition table; and

using the register definition file to create in silicon the registers of the ASP.

Claim 1 of the '774 patent teaches a method of operating a computer system to design an application specific processor (ASP) (CL21, L2-4); comprising:

defining a set of peripherals for the ASP which are responsive to stimuli and which communicate with a processor (CL21, L5-6);

generating for each peripheral an input file which defines the functional attributes of that peripheral in a high level language with an input data structure (CL21, L7-9);

entering the input file into the computer system and operating a modelling tool loaded on the computer system (CL21, L10-12).

Claim 1 of the '774 patent does not teach operating a modelling tool loaded on the computer system to generate from the input file a register definition file by allocating specific elements of the input data structure to predefined sectors of a register definition table; and using the register definition file to create in silicon the registers of the ASP. Claim 2 of the '774 patent teaches operating a modelling tool loaded on the computer system to generate from the input file a register definition file by allocating specific elements of the input data structure to predefined sectors of a register definition table (CL21, L26-30); and using the register definition file to create in silicon the registers of the ASP (CL21, L30-31). It would have been obvious to one of

ordinary skill in the art to arrive at Claim 1 of the application from the elements of claim 1 and 2 of the '774 patent since it requires only rearranging the limitations involved and paraphrasing them.

5. Claim 2 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1 and 2 and the descriptions of U.S. Patent No. 6,697,774. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Claim 2 teaches a method according to claim 1, wherein each input file comprises a data structure which defines for each of a set of registers the name of an element in the register, the bit length of the element, the functional status of the element and the function of the element.

Claims 1 and 2 of the '774 patent teach a method according to claim 1 as explained in Paragraph 4 above. Claims 1 and 2 of the '774 patent do not teach that each input file comprises a data structure which defines for each of a set of registers the name of an element in the register, the bit length of the element, the functional status of the element and the function of the element. Description in the '774 patent teaches that each input file comprises a data structure which defines for each of a set of registers the name of an element in the register, the bit length of the element, the functional status of the element and the function of the element (CL6, L25-27; CL6, L42-55). It would have been obvious to one of ordinary skill in the art to arrive at Claim 2 of the application from the elements of claim 1 and 2 and the description of the '774 patent since it

requires only rearranging the limitations involved and paraphrasing them and adding some limitations from the description.

6. Claim 3 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1 and 2 and the descriptions of U.S. Patent No. 6,697,774. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Claim 3 teaches a method according to claim 1, wherein each register definition table includes at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element.

Claims 1 and 2 of the '774 patent teach a method according to claim 1 as explained in Paragraph 4 above. Claim 2 of the '774 patent teaches that each register definition table includes at least predefined sectors (CL21, L29-30). Claims 1 and 2 of the '774 patent do not teach that each register definition table includes at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element. Description in the '774 patent teaches that each register definition table includes at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element (CL6, L25-27; CL6, L42-55). It would have been obvious to one of ordinary skill in the art to arrive at Claim 3 of the application from the elements of claim 1 and 2 and the description of the '774

patent since it requires only rearranging the limitations involved and paraphrasing them and adding some limitations from the description.

7. Claim 4 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1 and 2 and the descriptions of U.S. Patent No. 6,697,774. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Claim 4 teaches a method according to claim1, wherein the register definition table includes the word location of the register within a memory map for access during simulation of the ASP.

Claims 1 and 2 of the '774 patent teach a method according to claim 1 as explained in Paragraph 4 above. Claims 1 and 2 of the '774 patent do not teach that the register definition table includes the word location of the register within a memory map for access during simulation of the ASP. Description in the '774 patent teaches that the register definition table includes the word location of the register within a memory map for access during simulation of the ASP (CL6, L46-47). It would have been obvious to one of ordinary skill in the art to arrive at Claim 4 of the application from the elements of claim 1 and 2 and the description of the '774 patent since it requires only rearranging the limitations involved and paraphrasing them and adding some limitations from the description.

8. Claim 5 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 6 and 2 of U.S. Patent No. 6,697,774. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Claim 5 teaches a computer system which comprises a processor and a memory, the memory holding a program representing a modelling tool for use in designing an application specific processor (ASP), wherein the computer system comprises an input means for receiving a plurality of input files, each input file defining the functional attributes of a peripheral for the ASP in a high level language within an input data structure;

the processor being operable to execute the program representing the modelling tool to generate from the input file a register definition file by allocating specific elements of the input data structure to predefine sectors of a register definition table; and

wherein the computer system further comprises an output means for outputting the register definition file in a manner which is usable to create in silicon the registers of the ASP.

Claim 6 of the '774 patent teaches a computer system which comprises a processor and a memory, the memory holding a program representing a modelling tool for use in designing an application specific processor (ASP), wherein the computer system comprises an input means for receiving a plurality of input files, each input file defining the functional attributes of a peripheral for the ASP in a high level language within an input data structure (CL21, L48-55);

the processor being operable to execute the program representing the modelling tool (CL21, L56-58); and

the computer system further comprises an output means (CL22, L1-2).

Claim 6 of the '774 patent does not teach the modelling tool to generate from the input file a register definition file by allocating specific elements of the input data structure to predefine sectors of a register definition table; and an output means for outputting the register definition file in a manner which is usable to create in silicon the registers of the ASP. Claim 2 of the '774 patent teaches the modelling tool to generate from the input file a register definition file by allocating specific elements of the input data structure to predefine sectors of a register definition table; and an output means for outputting the register definition file in a manner which is usable to create in silicon the registers of the ASP (CL21, L26-31). It would have been obvious to one of ordinary skill in the art to arrive at Claim 5 of the application from the elements of claim 6 and 2 of the '774 patent since it requires only rearranging the limitations involved and paraphrasing them.

9. Claim 6 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 6, 2 and 7 of U.S. Patent No. 6,697,774. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Claim 6 teaches a computer system according to claim 5, wherein the input means comprises means for receiving a physical recording device holding the input file for each peripheral.

Claims 6 and 2 of the '774 patent teach a computer system according to claim 5 as explained in Paragraph 8 above. Claims 6 and 2 of the '774 patent do not teach that the input means comprises means for receiving a physical recording device holding the input file for each peripheral. Claim 7 of the '774 patent teaches that the input means comprises means for receiving a physical recording device holding the input file for each peripheral (CL22, L6-8). It would have been obvious to one of ordinary skill in the art to arrive at Claim 6 of the application from the elements of claim 6, 2 and 7 of the '774 patent since it requires only rearranging the limitations involved and paraphrasing them.

10. Claim 7 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 6, 2 and 8 of U.S. Patent No. 6,697,774. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Claim 7 teaches a computer system according to claim 5, wherein the output means comprises means for loading the register definition file onto a physical recording device.

Claims 6 and 2 of the '774 patent teach a computer system according to claim 5 as explained in Paragraph 8 above. Claims 6 and 2 of the '774 patent do not teach that the output means comprises means for loading the register definition file onto a physical recording device. Claim 8 and claim 2 of the '774 patent teach that the output means comprises means for loading the register definition file onto a physical recording device (CL22, L9-10; CL21, L26-30). It would have been obvious to one of ordinary skill in the art to arrive at Claim 7 of the application

from the elements of claims 6, 2 and 8 and the description of the '774 patent since it requires only rearranging the limitations involved and paraphrasing them.

11. Claim 8 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 11 and 1 of U.S. Patent No. 6,697,774. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Claim 8 teaches a computer program product stored on a computer readable medium and comprising software code portions operable when executed by a computer to read an input file which defines in an input data structure the functional attributes of a peripheral for an application specific processor in a high level language, and to generate from that input file a register definition file, the software code portions including a code portion for allocating specific elements of the input data structure to predefined sectors of a register definition table for each of a plurality of registers.

Claim 11 of the '774 patent teaches a computer program product stored on a computer readable medium and comprising software code portions operable when executed by a computer to read an input file (CL22, L34-37); and

generating from that input file a register definition file, the software code portions including a code portion for allocating specific elements of the input data structure to predefined sectors of a register definition table for each of a plurality of registers (CL22, L50-53).

Claim 11 of the '774 patent does not teach that an input file defines in an input data structure the functional attributes of a peripheral for an application specific processor in a high level language. Claim 1 of the '774 patent teaches that an input file defines in an input data structure the functional attributes of a peripheral for an application specific processor in a high level language (CL21, L7-9). It would have been obvious to one of ordinary skill in the art to arrive at Claim 8 of the application from the elements of claims 11 and 1 of the '774 patent since it requires only rearranging the limitations involved and paraphrasing them.

12. Claim 9 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 11 and descriptions of U.S. Patent No. 6,697,774. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Claim 9 teaches a register definition file stored on a computer readable medium and comprising a plurality of register definition tables, each table including at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element, and each table further including the word location of the register within a memory map for access during simulation of an ASP implementing the registers.

Claim 11 of the '774 patent teaches a computer program product stored on a computer readable medium and a register definition file (CL21, L48-55). It is obvious that the register

definition file could also be stored on a computer readable medium as the computer has means for loading the files on to a physical recording device.

Claim 11 of the '774 patent does not teach a register definition file comprising a plurality of register definition tables, each table including at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element, and each table further including the word location of the register within a memory map for access during simulation of an ASP implementing the registers. Description of the '774 patent teaches a register definition file comprising a plurality of register definition tables, each table including at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element (CL6, L25-27; CL6, L42-55); and each table further including the word location of the register within a memory map for access during simulation of an ASP implementing the registers (CL6, L46-47). It would have been obvious to one of ordinary skill in the art to arrive at Claim 9 of the application from the elements of claims 11 and description of the '774 patent since it requires only rearranging the limitations involved and paraphrasing them and adding some limitations from the description.

Response to Arguments

12. Applicant's arguments filed on July 23, 2004 have been fully considered.

Claim rejection under 35 U.S.C. §102 and 103 (a) are withdrawn in response to the applicant's arguments. New claim rejections under double patenting have been included in this office action. This office action is made non-final.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043, till October 27, 2004 and 571-272-3717 after October 27, 2004. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704, till October 27, 2004 and 571-272-3716 after October 27, 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
September 22, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER